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TOPICAL REVIEW

Silicon single-electron devices

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Abstract

Single-electron devices (SEDs) are attracting a lot of attention because of their capability of manipulating just one electron. For their operation, they utilize the Coulomb blockade (CB), which occurs in tiny structures made from conductive material due to the electrostatic interactions of confined electrons. Metals or III–V compound semiconductors have so far been used to investigate the CB and related phenomena from the physical point of view. However, silicon is preferable from the viewpoint of applications to integrated circuits because, on a silicon substrate, SEDs can be used in combination with conventional complementary metal-oxide-semiconductor (CMOS) circuits. In addition, the well established fabrication technologies for CMOS large-scale integrated circuits (LSIs) can be applied to making such small structures. LSI applications of the silicon SEDs can be categorized into two fields: memory and logic. Many kinds of device structure and fabrication process have been proposed and tested for these purposes. This paper introduces the current status of silicon-based SED studies for LSI applications.

Contents

1. Introduction

1.1. Si single-electron devices for future integrated circuits

Complementary metal-oxide-semiconductor (CMOS) technology will face significant technological limitations shortly after 2010 [1], and intensive studies are being conducted in computational architecture, circuit design and device fabrication to find ways to overcome this impending crisis. The major problem is that rapidly increasing power dissipation due to ever larger numbers of transistors and high levels of interconnections is pushing CMOS circuits beyond their cooling limit. This points to the need for some drastic change in how we build large-scale integrated circuits (LSIs), either on the system architecture, or base device level, or both. Roughly speaking, achieving low power operation of LSIs requires that we reduce the total capacitance of circuits and operation voltage, which means we have to reduce the number of electrons participating in the operation of some unit instruction. Single-electron devices (SEDs) [2–4], which literally have potential to manipulate electrons on the level of elementary charge, are thus considered to be the devices that will allow such a change. In addition to their low-power nature, SEDs have a rather simple operation principle, and because of this, operation is basically guaranteed even when device size is reduced to the molecular level. In addition, their performance improves as they become smaller. These properties are quite beneficial for large-scale integration. Also, SEDs can work not only as simple switches, but also have high functionality. Many theoretical works have been done to evaluate the possibility of building SED-based LSIs, and fundamental computational capability has already been proved.

SEDs can be made from any conducting material. Metals and III–V compound semiconductors have been employed since the very early stage of SED study in order to investigate the basic physics of the transport and to explore possible applications. Research aiming at the practical use of SEDs has also begun, and for this purpose, Si is mainly used. The benefit of using Si as a base material is, of course, that we can apply the existing advanced fabrication technologies for CMOS. Using such technologies, as will be described later, we have already shown the possibility of overcoming some fundamental difficulties in size control and stable operation of extremely small devices. In addition, the use of Si enables us to study combined SED–MOSFET (metal-oxide-semiconductor field-effect transistor) structures. This promises to produce new useful functions, some of which have already been demonstrated.

In this article, after briefly explaining the operation principles of SEDs right below, we will discuss, in the next section, SED fabrication using Si. We will see that the Si-based technology enables us to fabricate very small SEDs in a controlled way, and that one of the fundamental problems, the so-called offset charge problem, might be solvable. These are the major outputs of the studies on Si-based SED fabrication. Section 3 describes SED applications to memory. Memory is the area where SEDs are expected to emerge for practical use first. The possibility of room-temperature operation and large-scale integration was first shown in this area. A variety of proposed structures will be presented for both dynamic and static memories. Applications to logic are attractive and a considerably large number of logic styles have been proposed. Although the integration level is quite low, some fundamental circuits have been successfully

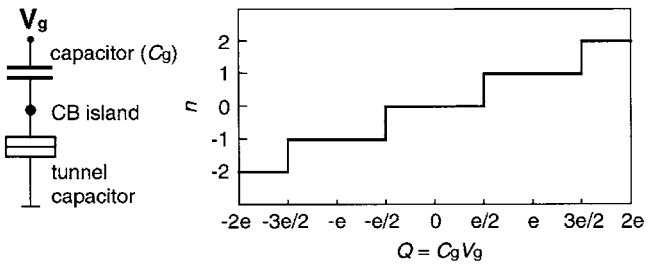

Figure 1. Equivalent circuit and stability diagram of a single-electron box. In the diagram, n is the electron number in the island, and Q and V_g are the external charge and voltage to the normal capacitor with a capacitance C_g.

fabricated. These studies will be covered in section 4. Section 5 concludes the article with mention of some future prospects of SEDs.

1.2. Operation principle of single-electron devices

Likharev [4] has already written a nice review of the physics and possible applications of SEDs. We here therefore briefly describe only their basic operation principles. The basic mechanisms to ensure the manipulation of a single electron are the Coulomb blockade (CB) and single-electron tunnelling [5]. (In the literature, a single-electron device or SED is generally a device that uses these phenomena. However, there are other devices that enable the manipulation of an elementary charge. In addition, some devices and circuits handle a bunch of electrons (not only one) and the CB and single-electron tunnelling are not always the basic mechanisms of their operation. In this review, we refer to such non-CB-based devices as SEDs as well.)

The SEDs comprise small conducting materials called the CB islands (or simply islands or quantum dots) and tunnel capacitors (also called tunnel junctions), which are special capacitors that allow quantum mechanical tunnelling of electrons. The simplest SED is the so-called single-electron box [2, 4], which has one CB island and one tunnel capacitor. Its equivalent circuit and stability diagram are shown in figure 1. In the equivalent circuit, the double box symbolizes the tunnel capacitor and the region between the tunnel capacitor and the normal capacitor corresponds to the CB island. The CB island can be made using any material (metals, semiconductors and even some molecules) as long as it is conductive. When the CB island is sufficiently small, the charging energy E_c for adding one electron to the island becomes large. E_c corresponds to a half of the energy gap between two energy levels, of which the electron numbers in the island differ by unity. In such a case, an additional electron is prohibited from entering the island through the tunnel capacitor unless the potential of the island is lowered by an external bias. This phenomenon is known as the CB. As indicated by the stability diagram, the number of electrons increases one by one as the bias increases. The single-electron box is unstable at the transition points where the single-electron tunnelling occurs. This single-electron box is a basic structure for single-electron memories, and some derivatives will be shown in the next section.

The most fundamental three-terminal SED, which is called the single-electron transistor (SET) [6–9], is illustrated in figure 2. The SET also has one CB island but it has another tunnel capacitor and voltage source. The electrode with the normal capacitor is the gate, and the other two electrodes are the source and drain. As in the single-electron box, the electron number in the island is controlled by external biases, as shown in the stability diagram. The double-hatched rhombic-shaped regions, which are called Coulomb diamonds,

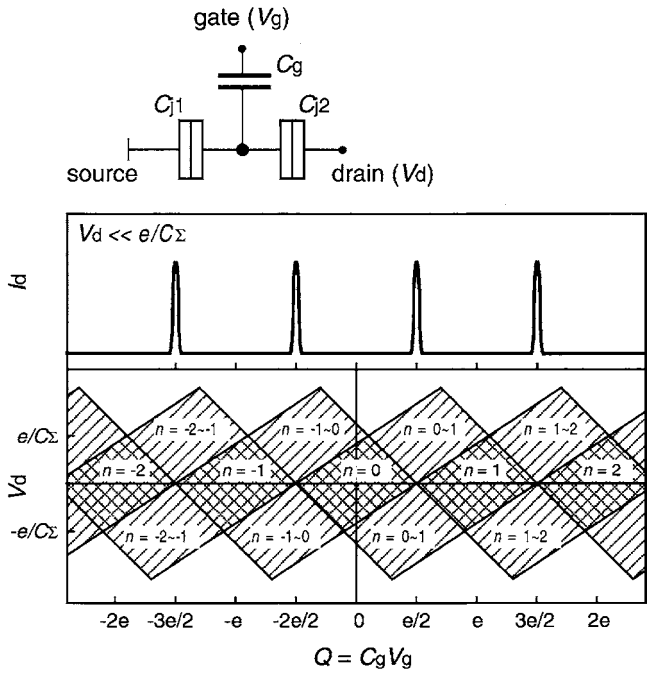

Figure 2. Equivalent circuit, drain current characteristics and stability diagram of a SET. I_d and V_d are the drain current and drain voltage. Q and V_g are the external charge and voltage to the gate with a capacitance C_g. C_Σ is the total capacitance of the island, which is the sum of C_g and the two junction capacitances, C_{j1} and C_{j2}.

are the stable regions. Outside the Coulomb diamonds, the number of electrons in the island fluctuates between certain numbers. The degree of the fluctuation is related to how far the voltage conditions are apart from the Coulomb diamonds. In the single-hatched regions, the fluctuation is minimum, i.e., the electron number changes only between two adjacent integers. In these regions, when there is a finite voltage between the source and drain, electrons are transferred one by one between the two electrodes. If we scan the gate voltage with a fixed small source–drain voltage, the CB states and the single-electron tunnelling states appear by turns and the drain current versus gate voltage characteristics exhibit multi-peak structure, as shown in the figure. This is called the CB oscillation. The shape and the size of the Coulomb diamonds are determined only by the gate and junction capacitances. For example, the maximum drain voltage for CB is given by e/C_Σ, where $C_\Sigma = C_g + C_{j1} + C_{j2}$ is the total capacitance of the island, and C_g, C_{j1} and C_{j2} are the gate capacitance and junction capacitances, respectively.

There are two criteria for observing the above-mentioned properties. One is that the resistance of the tunnel capacitor must be sufficiently larger than the quantum resistance $R_q = h/e^2$ ($\sim$25.8 kΩ). Otherwise, the number of electrons in the island fluctuates because of the uncertainty relationship even in the CB regions. The other is that the charging energy E_c must be larger than the thermal energy. Otherwise, heated electrons tunnel through the barriers and the CB does not occur. (For example, as the temperature rises, the current peaks in figure 2 become broaden, and finally blur out.) This relation is expressed as $E_c = e^2/(2C_\Sigma) > kT$. When the island is assumed to be a sphere with a diameter d and embedded in a dielectric material with a dielectric constant ε, the self-capacitance (nearly equal to C_Σ) is given by

$2\pi\varepsilon_0\varepsilon d$. Thus, a smaller island results in a higher E_c, and in the operation at a higher temperature. For room-temperature ($kT = 25.9$ meV) operation, d should be less than 14 nm in the case of SiO_2 dielectrics ($\varepsilon = 3.9$). The size control of such a small structure is a technological challenge in Si-based SEDs.

There are some derivatives of single-electron boxes and SETs. Their multi-tunnel junction versions and multi-gate versions are examples. These have high functionality and will be introduced in the following sections.

It should also be noted that there is another type of SET, called the resistive SET or R-SET [8]. In the R-SET, the gate is connected to the island via a resistor instead of a capacitor. Although the R-SET has some advantages [8], very few studies have so far been done either numerically [10] or experimentally [11] due to difficulty in fabrication. Thus, the R-SET is not discussed in the following sections. The SET shown in figure 2 is sometimes called the capacitive SET or C-SET in order to distinguish it from the R-SET. We hereafter refer to the C-SET simply as the SET.

2. Fabrication of Si single-electron transistors

The research on SET fabrication started with metals or superconductors and then expanded to semiconductors. The first experimental demonstration of SETs was done with metal/oxide system in 1987 [6, 7]. The pioneering work on Si SETs was done in 1989 by Scott-Thomas *et al* [12, 13], which also reported the first observation of CB oscillation in semiconductors. The observed CB oscillation in conductance was attributed to Si islands unintentionally formed in a narrow one-dimensional channel in a double-gate Si MOSFET. In 1991, similar characteristics were observed in a double-gate Si MOSFET with a point contact [14]. Before that, in 1990, Meirav *et al* [15] reported on a SET fabricated with a GaAs/AlGaAs two-dimensional electron-gas system. The operating temperature of these early-era SETs was below 1 K because the CB islands were not small enough. Because this temperature was high enough for physics research, there have been many reports on mesoscopic physics of quantum dots formed in a two-dimensional electron-gas system of compound semiconductors, over the last ten years.

In contrast, from the viewpoint of application to practical Si LSIs, the operating temperature of 1 K is too low. To date a variety of fabrication processes for Si-based SETs have been proposed and the characteristics of the fabricated devices have been examined. Most of these studies aimed at high-temperature operation of SETs, typically above 4 K to room temperature. The required size of Si CB islands is of the order of 10 nm or less, which is comparable to a few tens of times the lattice constant of Si crystal. It is not easy to fabricate such small Si islands with good reproducibility. Historically speaking, the research on Si SETs has focused on achieving high-temperature operation of SETs and this still remains the challenge.

Before reviewing the specific methods of fabricating Si SETs, a few important aspects of SET fabrication should be addressed. One is, of course, island size reduction. For example, to obtain E_c of 260 meV, which is ten times the room-temperature thermal energy, the C_Σ of the Si island has to be 0.3 aF, which corresponds to $d = 1.4$ nm for the spherical island surrounded by the SiO_2. In such a small Si island, the energy separation due to the quantum-size effect is expected to appear and relax the requirement for shrinking the island size. Another point is the attachment of two tunnel junctions to such a small island, and with what material. Low tunnel resistance is preferable for achieving reasonable derivability, though it is theoretically limited by R_q. Lastly, there is control of the size and the position of Si islands with good reproducibility. From the viewpoint of LSI application, the device fabrication method must have sufficiently good controllability and reproducibility.

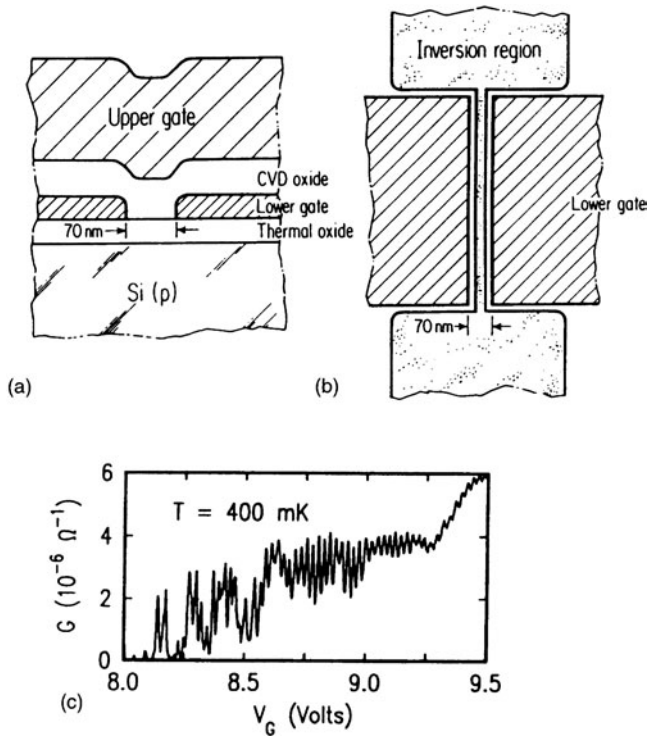

Figure 3. (a) Schematic cross section and (b) top view of the first reported Si SET, which was fabricated using double-gate MOS structures. (c) Measured conductance as a function of the gate voltage. The CB oscillation was observed at 400 mK. Reprinted with permission from [10]. Copyright 1989 by the American Physical Society.

2.1. Island formation by lithography

Lithography is the most direct way of forming miniaturized structures. It also has the merit of compatibility with present LSI technology. Nevertheless, it is not easy to form a quasi-isolated Si island because it requires three-dimensional confinement. To understand the situation, consider the first reported Si SET that used a double-gate MOSFET [12]. The device structure and electrical characteristics are shown in figure 3. In this device, a narrow one-dimensional channel is formed in the Si inversion layer. The use of the inversion layer is the simplest way to achieve vertical confinement, though the confinement is rather weak. The lateral confinement was electrically introduced using a narrow gap (<100 nm) opened in the lower gate by x-ray lithography. The final confinement, that is, the formation of tunnel barriers, is due to electrostatic potential originating from random charged impurities. Due to the random formation of tunnel barriers, the island is neither small enough ($E_c < 1$ meV) nor controllable from the practical point of view. To gain better controllability, Matsuoka *et al* [16] introduced crossbar gates to electrically form tunnel barriers in the Si channel and reported multiple-island SETs having E_c of a few milli-electron volts.

A promising way to further reduce the island size is to use a two-dimensional silicon-on-insulator (SOI) layer of separation-by-implanted-oxygen (SIMOX) or bonded wafers, instead of bulk Si wafers. Since SiO_2 has a much larger bandgap energy (9 eV) than Si (1.1 eV), strong physical confinement is possible. The use of SOI wafers in SET fabrication was first reported

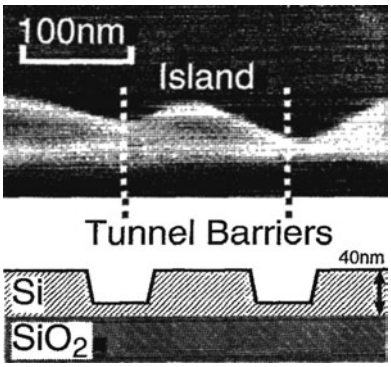

Figure 4. SEM image of the Si island in a one-dimensional Si wire on a SOI wafer, and a schematic diagram. Reprinted with permission from [15]. Copyright 1994 American Institute of Physics.

by Ali and Ahmed [17]. A scanning electron microscope (SEM) image of the device and its schematic diagram are shown in figure 4. They made a uniform one-dimensional Si wire by electron beam (EB) lithography and dry etching. Then, two narrower parts were formed in the Si wire by a second EB lithography and etching. These parts were expected to act as tunnel barriers due to the quantum-size effect. The obtained E_c was 1.6 meV and not much higher than that of SETs on bulk wafers since the island size was still limited by the lithography. The CB effect was observable up to a few kelvin.

The first observation of the CB oscillation at room temperature was made by Takahashi *et al* [18–21], who used a fabrication process called pattern-dependent oxidation (PADOX). The process is simple: it is the thermal oxidation of a short Si wire, whose two ends are connected to wide Si layers. Thermal oxidation of Si is one of the most stable processes in LSI technology. It is widely known that the oxidation of Si depends on mechanical stress accumulating due to the volume expansion during the oxidation [22]. Since the influence of oxidation-induced stress becomes enormous when a nanometre-scale Si structure is oxidized [23, 24], how the oxidation proceeds is strongly dependent on the initial Si pattern. Schematic diagrams of the device structure are shown in figures 5(a) and (b). The initial Si wire was defined in a SOI layer by EB lithography and dry etching and was 30 nm wide, 30 nm high and 30–100 nm long. Next, it was thermally oxidized in a dry oxygen ambient. Then, polysilicon gate was formed over the Si wire. The electrical measurement of the device with the oxidized Si wire revealed that a Si island was effectively formed in the Si wire. The temperature dependence of the current–gate voltage characteristics is shown in figure 5(c). E_c was found to range from 10 to 50 meV, which was larger than the previously obtained E_c by more than one order of magnitude. The largest E_c corresponds to a 7 nm diameter Si island with $C_\Sigma = 1.5$ aF. Such a small dimension, which is below the lithographic limit, is possible because the size of the remaining Si is reduced as oxidation proceeds. This is one of the big advantages of thermal oxidation.

Another important feature of PADOX is that C_g of the Si island showed an almost linear relation to the designed length of the Si wire [19], which was the first experimental datum demonstrating the reproducibility of Si SET fabrication. The result is shown in figure 6. This strongly suggests that PADOX converts a Si wire to a Si island with two tunnel barriers at both ends in a self-aligned manner. However, the result was surprising because the oxidized Si wire was still continuous between the Si pad layers and there was no constricted region in the Si wire. To explain the origin of the tunnel barriers, a model was proposed that takes into account

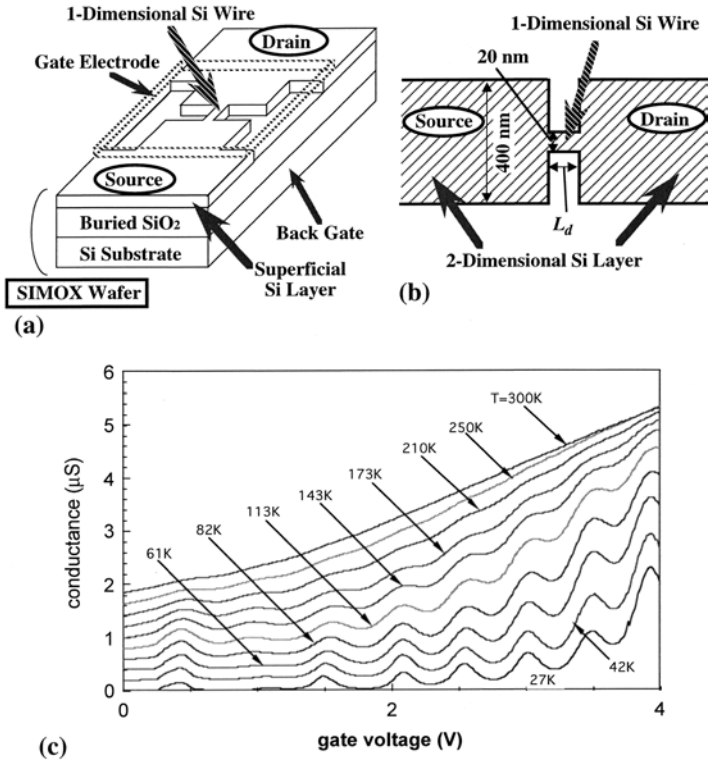

Figure 5. (a) Schematic diagram and (b) top view of the EB pattern of a Si SET fabricated by PADOX [16, 17]. (c) Temperature dependence of conductance oscillation of the SET; the CB oscillation was observed up to room temperature.

the bandgap modulation of Si due to the quantum confinement and the oxidation-induced stress [25]. A schematic diagram of the model is shown in figure 7. The model assumes that a single potential barrier (∼50 meV high) is formed as a result of the quantum size effect in the Si quantum wire. The compressive stress (∼20 000 atm) [23] accumulates in the middle of the wire. The compressive stress is expected to be lower around the ends of the Si wire because of the shear stress caused by the oxidation at the Si/buried oxide interface of Si pad layers. Since the compressive stress reduces the Si bandgap, the potential well (∼150 meV deep) is introduced at the middle of the barrier potential, resulting in the double-tunnel-barrier potential. This model significantly pointed to the importance of oxidation-induced stress in designing nanometre-scale Si devices. To confirm the model, however, further experimental investigation is necessary. An asymmetric potential profile of the tunnel barrier was suggested from the bias dependence of the conductance of the fabricated SET [26].

PADOX led us to expect that various SETs could be fabricated by designing the Si pattern appropriately. Recently, with the development of an improved version of PADOX called vertical-PADOX (V-PADOX) [27, 28], this indeed turned out to be true. V-PADOX utilizes the thermal oxidation of a relatively wide (>60 nm) Si wire with a thickness modulation. A diagram of the Si structure is shown in figure 8(a). A thin region with the length of 10–60 nm is sandwiched by the thicker regions. Thermal oxidation affects this structure in two ways. First, the two edges of the thin region of the Si wire remain as twin 10 nm size Si wires because the built-up stress suppresses their oxidation, whereas the centre part is completely oxidized.

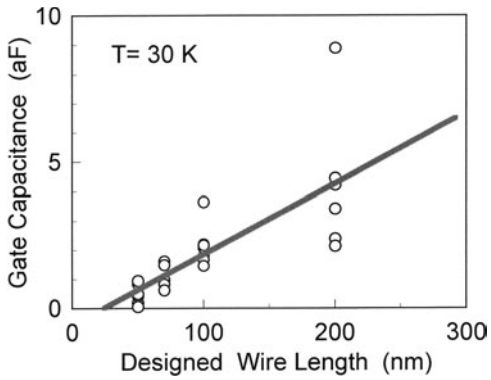

Figure 6. Relation between C_g and the designed length of the Si wire for the SET fabricated by PADOX.

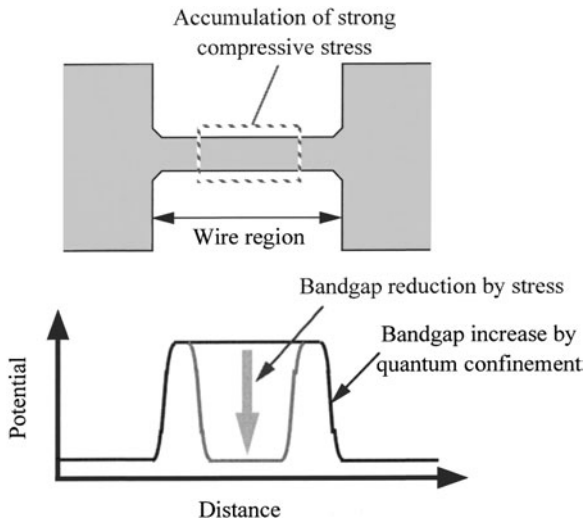

Figure 7. Oxidation-induced-stress model for the potential profile of the Si SET fabricated by PADOX.

The cross-sectional transmission electron microscope (TEM) image of the thin Si region is shown in figure 8(b). Secondly, tunnel barriers are formed at both ends of the twin Si wires, probably due to the same mechanism by which SETs are produced by PADOX. Consequently, twin SETs are formed at the same time, which is suitable for logic-circuit application. A clear relation between C_g of the Si island and the length of the thin Si region was observed, which is evidence of the self-aligning formation of Si islands.

Until now, there have been many reports on Si SETs with E_c larger than a few tens of meV, which was fabricated based on one-dimensional Si wires on a SOI wafer. Some of those reports focused on the effect of quantum confinement in the Si island because the size of the Si island is less than 20 nm. In several experiments, negative differential conductance was observed in the SET current [29–31] and its origin was discussed in terms of the nature of quantized energy levels. Leobandung *et al* reported a SET using a one-dimensional Si wire with two constrictions defined by lithography [32]. They observed CB oscillations with a gap energy of 40 meV, and estimated that about half of that was due to the CB effect and the

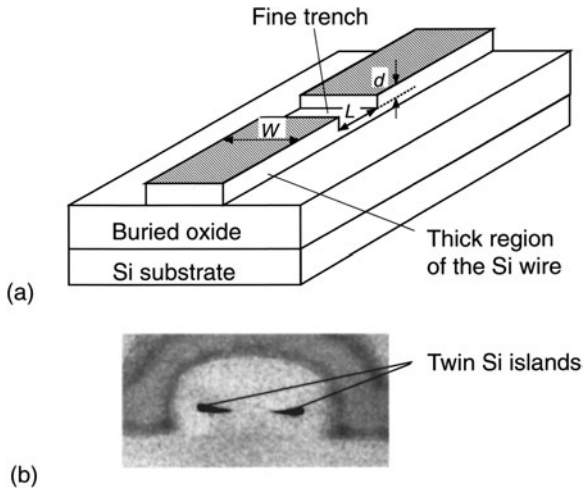

Figure 8. (a) Schematic view of the Si pattern used for SET fabrication by V-PADOX [25]. (b) Cross-sectional TEM image of the thin Si region.

other half was due to the energy between the quantized levels due to the confinement. They reported a single-hole transistor with a similar structure [33]. Ishikuro *et al* reported a SET using 10 nm wide and 100 nm long triangular Si wires [34]. Multiple-island structures were formed due to some unknown randomness in the Si channel. They also reported a SET with $E_c = 58$ meV and discussed the quantum-confinement effect in the Si island [29]. In this work, they employed a point contact defined by EB lithography and anisotropic etching. Since the device structure apparently did not include tunnel barriers, they suggested that the tunnel barrier formation is due to localized states or Si nanoparticles at interfaces, or PADOX. To get more information on the tunnel barrier, they investigated the characteristics of the electron and hole currents in the same channel by using a SET with both n- and p-type source/drain contacts [35]. The device structure and the measured electrical characteristics are shown in figure 9. They observed the CB oscillation for both types of operation and concluded that the tunnel barriers for both electrons and holes were formed. More recently, the same group reported fabrication of a similar point-contact SET with gate oxide by chemical vapour deposition (CVD), not by thermal oxidation [36]. They insisted on the possibility of mechanisms other than oxidation-induced stress in PADOX.

As described above, it was widely recognized that SETs based on Si wires could provide high-temperature operation. However, there are also other issues. A major one is how to make SETs with good reproducibility, especially concerning tunnel barrier formation. There are many candidates for the origin of the potential modulation in a Si wire, such as quantum confinement, mechanical stress, a gate-induced electric field and ionized impurities. Even if the CB oscillation is successfully observed in some structure designed to produce tunnel barriers, it might be due to some unexpected mechanism. We emphasize the importance of obtaining a clear relation between the electrical characteristics and the structure parameters, which will guarantee the controllability of the fabrication process. At present PADOX and V-PADOX are the most promising methods in this respect. Although they are reproducible to a certain extent, the mechanism of the tunnel-barrier formation has not been completely clarified and is still controversial. They also need further investigation to improve size reduction. Very recently, Kim *et al* [37, 38] showed data demonstrating reproducibility in a SET fabrication

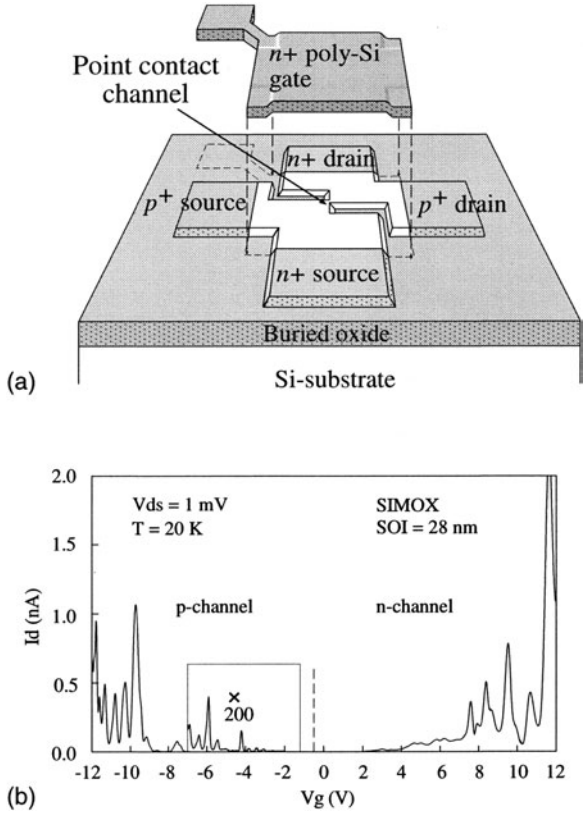

Figure 9. (a) Schematic view of the SET using a point-contact MOSFET with n^+ and p^+ source/drain contacts. (b) Current as a function of the gate voltage for both-types of channel. Reprinted with permission from [33]. Copyright 1999 American Institute of Physics.

where the tunnel barriers are electrically formed by the sidewall depletion gates. A sketch of the device structure and the measured electrical characteristics are shown in figure 10. In the devices, C_g was controlled by the distance between the two depletion gates. This fabrication process might be another promising approach because the tunnel barrier would be controlled in a simpler way.

Another issue is how to control the quantum-size effect in ultrasmall Si islands. This could be problem from the practical point of view because it likely introduces some complex irregularity in the CB oscillation, which is periodical in the case of metal-based SETs. One approach to avoid such a complex feature might be the use of doped Si wires on SOI wafers. Many groups have reported SETs based on doped Si wires [39–43]. Some of them utilized multiple-island structures originating from the random fluctuation in a Si wire, which might be related to the doping level or in the wire width [39, 40]. Another reported rather periodical CB oscillations similar to those of SETs with a single metal island [41–43]. This might indicate that the doping is useful in getting a periodical CB oscillation, although the E_c values of these SETs were less than 15 meV and not large enough to be strongly affected by the quantum confinement. It should be noted that an undoped SET with a similar E_c also showed a rather periodic CB oscillation [18], expect for the few-electron regime where the electron number in the Si island is small. Investigating the quantized energy states in an ultrasmall Si dot

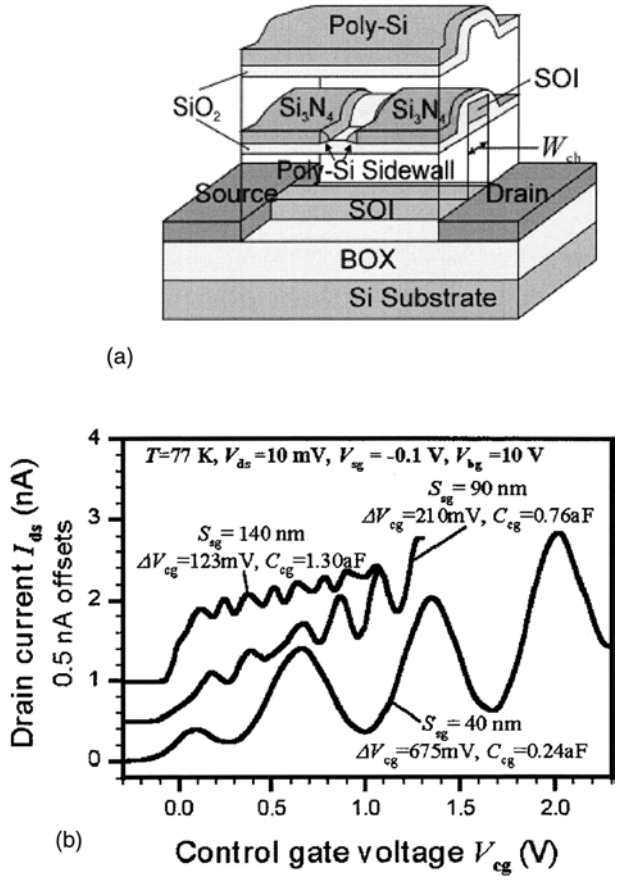

Figure 10. (a) Schematic diagram of the SET with sidewall depletion gates on a SOI wire. (b) Current as a function of the gate voltage for SETs for various space distances between the two depletion gates. Reprinted with permission from [36]. Copyright 2002 IEEE.

and the effect of the doping is an important subject. We should add that negative differential conductance, probably caused by the quantum-confinement effect, might be useful in some circuit application.

In addition to SOIs, polysilicon may offer much flexibility of fabrication. Ohata *et al* [44] reported SET fabrication using a lithographically defined structure. A polysilicon island was first fabricated by patterning a deposited polysilicon layer. After thermal oxidation to form SiO_2 tunnel barriers, two polysilicon leads were attached to the island. Though the observed E_c of around 10 meV did not completely equal the estimated value expected from the physical size, this kind of approach is straightforward and should be explored more. In polysilicon nanostructures, grain boundaries may play some role in the electron transport. The possibility that a grain boundary acts as a tunnel barrier was discussed on the basis of multiple-island characteristics observed in a doped polysilicon wire [45].

2.2. Natural island formation by nucleation or random fluctuation

As a method not relying on lithography, nucleation of Si islands (often called Si nanocrystals) has been widely investigated. The most attractive feature of Si nanocrystals is that we can make

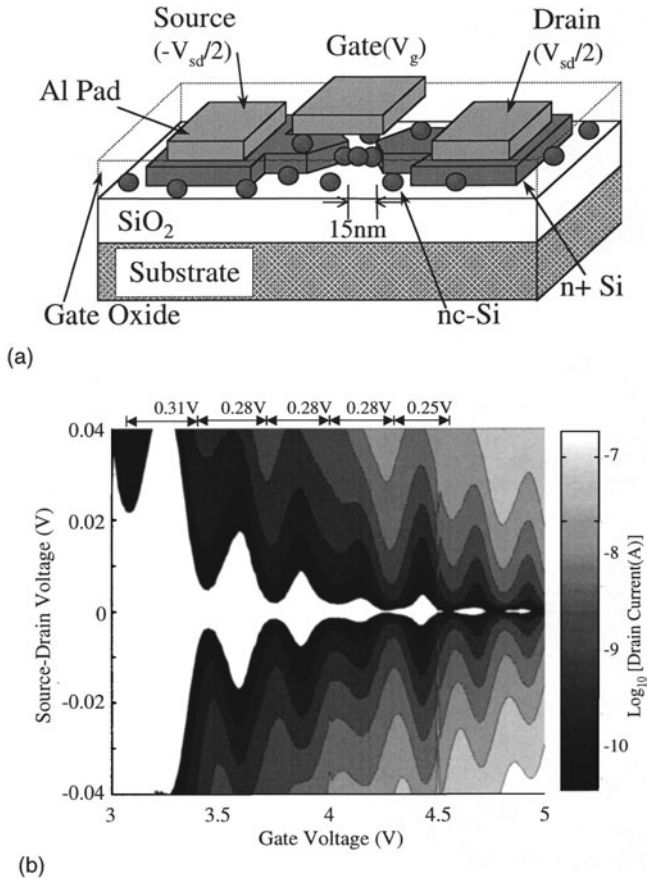

Figure 11. (a) A schematic of the SET using Si nanocrystals. (b) Drain current contour plot in the gate voltage and drain voltage plane at 20 K. White-coloured CB regions designate current <10 pA. Reprinted with permission from [47]. Copyright 2000 Japan Society of Applied Physics.

use of Si islands with well defined shapes. Tunnel current through a single Si nanocrystal on the substrate was measured with an atomic force microscope with a conductive tip. The observation of negative differential conductance [46] and Coulomb staircases [47] was reported. Dutta *et al* [48, 49] reported SETs using Si nanocrystals. The device structure and the measured electrical characteristics are shown in figure 11. Si nanocrystals about 8 nm in diameter were deposited on the substrate by means of VHF-plasma CVD, on which source and drain electrodes with a narrow gap had been formed. Several Si nanocrystals bridging the gap acted as CB islands. SET characteristics with E_c of a few tens of meV were observed. The most crucial issue in applying Si nanocrystals to SETs is how to put them at a desired place. Random deposition makes it difficult to fabricate SETs with the same parameters such as tunnel capacitance and resistance because the position of the Si island strongly affects them. Selective-deposition techniques might make accurate control of the island position possible.

Random formation of multiple Si islands in an ultrathin layer is another simple way to make islands without nanometre-scale lithography. The pioneering work of single-electron memories was performed with a thin polysilicon layer, which will be described in section 3. Uchida *et al* [50] took a similar approach to the SET fabrication, but used a thin SOI layer. They introduced a nanometre-scale undulation in a 3 nm thick SOI layer by a chemical treatment.

They ascribed their obtained E_c of 35 meV to Si islands that formed as a result of fluctuations in the quantum-confinement energy due to SOI thickness variations. The merit of these methods based on natural and random formation is the ease with which they can provide nanometre-size Si islands. However, similar to Si nanocrystals, they are somewhat not oriented towards SET fabrication because of the lack of controllability in positioning the Si islands in a desired place. The methods described in this subsection are suitable for memory application, which will be described in section 3.

2.3. Comparison to single-electron transistors made from other materials

Si SETs have remarkable advantages compared with SETs made of other materials. One merit is that E_c larger than tens of meV is possible because of the sophisticated fabrication processes in Si technology. This also means that the Si SET fabrication can be highly compatible with conventional LSI technology. There have been several attempts to miniaturize a CB island made of other materials. Pashkin *et al* [51] fabricated Al/Al_2O_3 SETs by means of angled evaporation, a technique that is commonly used for metal SETs. They developed an oxidation process to shrink the island and reported E_c of 115 meV as their best data. Matsumoto *et al* [52] fabricated SETs with Ti/TiO_x systems. They employed an atomic-force-microscope- (AFM-) based oxidation technique to define islands and achieved E_c of a few tens of meV. GaAs-based SETs operating at relatively high temperature have been fabricated by applying a Schottky inplane-gate structure or wrap-gate structure to the two-dimensional electron gas system [53]. Based on these techniques, E_c of 14 meV was obtained using gated ridge-quantum-wire structures [54]. Very recently, SETs have been fabricated from carbon nanotubes, which have an E_c of 41 meV [55]. Although all these attempts indicate that materials other than Si may provide room-temperature-operating SETs, Si is now the most feasible because advanced LSI fabrication technology, which enables an accelerated down-scaling of CMOS, can be utilized for the SET fabrication.

The other important feature of Si SETs is their stable operation. It has been often said that a SET is very sensitive to charges and therefore so-called offset charges, or background charges, can change the characteristics of the device. The CB oscillation originates from the one-by-one change of the stable electron number in the CB island. The offset charges likely add a random phase offset to this oscillatory characteristic. If the offset is a large fraction of 1 e, the operation point of the SET changes significantly. This argument has led to a very pessimistic view regarding the practical use of SETs in electronic circuits [4]. It is widely known that metal-based SETs are indeed strongly influenced by mobile offset charges and thereby show a change in their electric characteristics in thermal cycling, or even during measurement when fixed temperature and voltages are applied to the device [56]. Recently, the long-term drift of Si SETs fabricated by PADOX was investigated. The devices showed a drift less than 0.01 e over some weeks [57]. This excellent stability is a very advantageous character of Si SETs.

In order to put Si SETs into real use, reproducible fabrication techniques must be established. Although circuit architectures are also of vital importance, as we will see in section 4, the base of the circuit is the device: fluctuation in the device characteristics should be reduced as much as possible. Extensive investigations have to be continued to attain a larger E_c and better controllability in SED fabrication.

3. Single-electron memory

Memory is the first and foremost application of silicon SEDs, and has been extensively researched. One reason this is so is that the SEDs can operate in smaller dimensions, and this

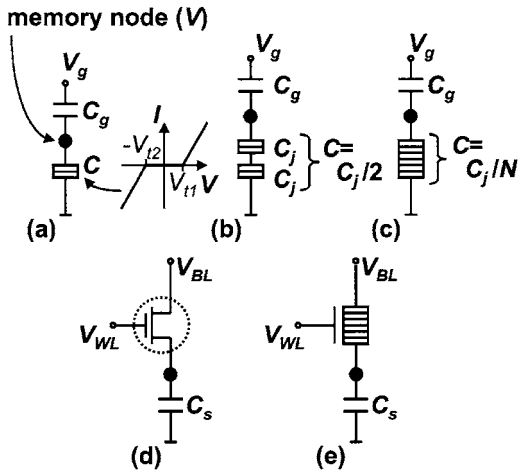

Figure 12. Various electron storage schemes used in single-electron memories. (a) A single-tunnel-junction electron box with non-linear tunnel resistance, (b) a double-tunnel-junction electron trap, (c) a MTJ electron trap, (d) a storage capacitor driven by a write/erase MOSFET and (e) a storage capacitor driven by a write/erase MTJ-SET. The term 'electron box' is used here to distinguish it from the 'electron trap'. The electron box does not have a memory effect in general.

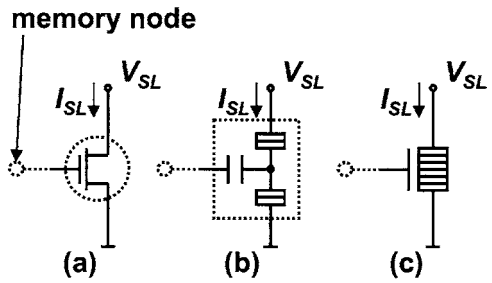

Figure 13. Various kinds of charge sensing device used in single-electron memories. (a) A MOSFET, (b) a SET and (c) an MTJ-SET.

directly leads to the increased memory density. Another is that memory usually has a periodic and simple structure, and this is expected to make the implementation of the emerging devices straightforward. The scaling limit in the current silicon memories, both flash memory [58] and dynamic random access memory (DRAM) [59], also adds to the demand for single-electron memories.

3.1. General structures

Most of the proposed single-electron memories are floating-node types, in which a limited number of electrons are stored in the floating memory node and the presence of the charge is detected by a charge-sensing device [4, 60]. SEDs can be used in either electron storage or charge sensing schemes. Since there are various versions of both schemes as shown in figures 12 and 13, possible combinations of them are numerous.

A distinctive device in electron storage schemes is the electron trap, which consists of two or more serial tunnel junctions and a capacitor (figures 12(b) and (c)). In the relationship between the potential of the memory node V and the gate voltage V_g (figure 14),

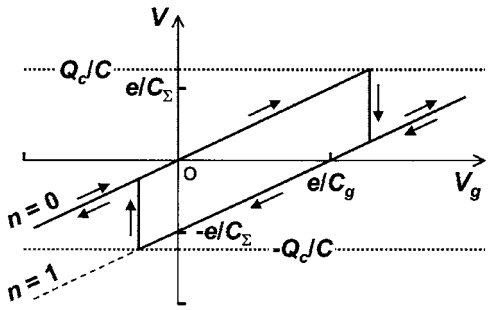

Figure 14. Potential of the memory node V as a function of gate voltage V_g for double- and multiple-tunnel-junction traps (figures 12(b) and (c)). Shown here is the bistable operation with the number of electrons n on the memory node equal to zero or one under the condition of $N = 2$ and $C_g/C = 3$.

tunnelling of the electron in and out of the memory node is prohibited by CB in the regime $-Q_c/C < V < Q_c/C$. The CB is effective as long as the leakage caused by co-tunnelling or thermal excitation can be ignored in the relevant timescale. The critical charge Q_c is given by [60]

$$Q_c = \frac{eC}{C_\Sigma}\left(\frac{1+\Delta}{2}\right). \tag{1}$$

Here, C_Σ is the total capacitance $C + C_g$, and Δ is given by

$$\Delta = \left(1 - \frac{1}{N}\right)\frac{C_g}{C} \tag{2}$$

where N is the number of serially connected tunnel junctions. As shown in figure 14, V increases with a slope of C_g/C_Σ until the boundary of the CB regime ($V = Q_c/C$) is reached, where an electron tunnels into the memory node and the V drops abruptly by e/C_Σ. Even if the V_g sweep is reversed, the electron is trapped until the sweep reaches the other boundary ($V = -Q_c/C$), where the electron tunnels out of the memory node. Thus, a hysteresis loop appears, and bistability is attained at $V_g = 0$ for $1 < \Delta < 3$. If V_g is further increased beyond the area shown in figure 14, more electrons can be transferred to the memory node, and multiple electrons ($n > 1$) can be stored at $V_g = 0$ by changing the capacitance parameters to satisfy $\Delta > 3$.

The stability of a trapped electron can be assessed by calculating the electrostatic energy of the system as a function of the position of an extra electron (figure 15) [4]. For the number of tunnel junctions more than one ($N > 1$), the curves become convex and an energy barrier appears between states with and without an extra electron in the memory node. This results in a stable storage of an electron in the node. As seen in figure 15, the increased number of tunnel barriers N has a limited effect in increasing the barrier height, but a large N is favourable for decreasing the co-tunnelling rate [61] and alleviating the effect of random offset charges [4].

Though, from an electrostatic energy point of view, stable storage cannot be attained with a single tunnel barrier ($N = 1$), quasi-stable storage is possible if the tunnel resistance is nonlinear. The Fowler–Nordheim tunnelling observed in MOS diodes is an example of nonlinear conduction. Here, we consider the current–voltage characteristics having threshold voltages V_{t1} and $-V_{t2}$ for simplicity (figure 12(a)). As shown in figure 16, V increases beyond the border of the CB regime ($V = e/2C_\Sigma$) until V_{t1} is reached, at which point an electron tunnels into the memory node and the V drops abruptly by e/C_Σ. In manner similar to that in

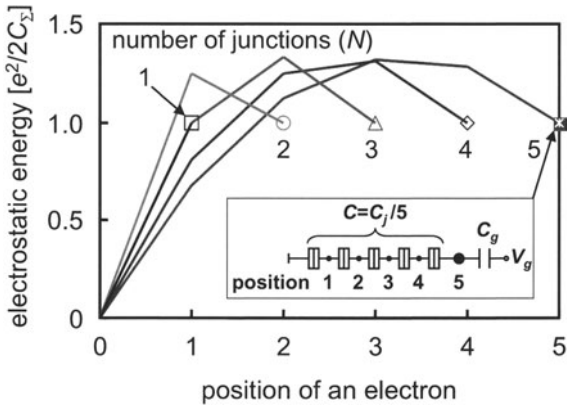

Figure 15. Electrostatic energy of the MTJ trap system with an extra electron as a function of its position when $V_g = 0$ and $C_g/C = 3$.

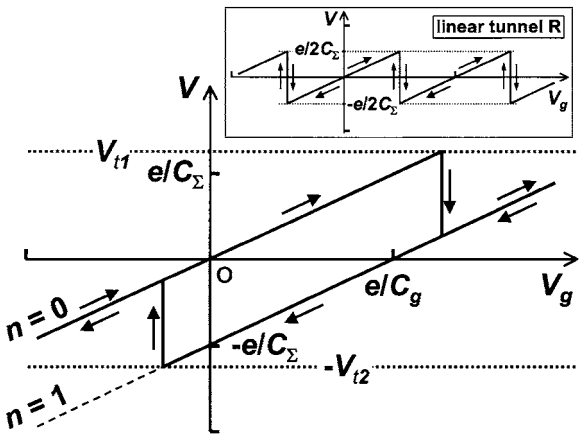

Figure 16. Potential of the memory node V as a function of gate voltage V_g for a single-tunnel-junction electron box with non-linear tunnel resistance (figure 12(a)). The inset shows the case for linear tunnel resistance without the memory effect.

multiple tunnel junctions (MTJs), a hysteresis loop appears for $V_{t1} + V_{t2} > e/C_\Sigma$, and bi- or multi-stability can be attained. This single-junction scheme is simple in structure, and widely seen in single- and multi-dot memories.

A discrete number of electrons in the memory node is an important feature of the single-electron memories, because this may lead to a quantized shift and a narrow distribution of device parameters, such as the threshold voltage of a charge-sensing device, and thus widen the manufacturing and operating margins.

Another electron storage scheme is based on a serially connected transistor and a storage capacitor (figures 12(d) and (e)). Since transistors are three-terminal devices, this scheme provides flexibility in memory operations. Serial connection of a transistor and a capacitor can be found in conventional DRAMs and is not specific to single-electron memories, but the number of stored electrons can be very small if an efficient charge sensing device is used with them.

Figure 13 shows the charge sensing devices seen in single-electron memories. Drain current is modulated by charges in the memory node, and thus the content of a memory can

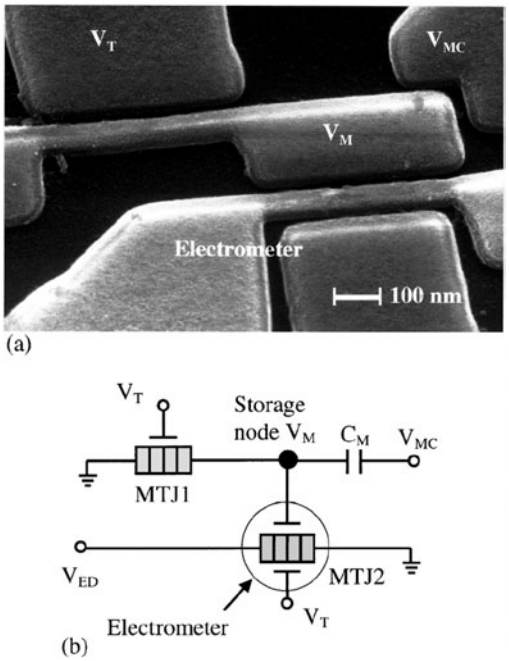

Figure 17. A memory with an MTJ electron trap and an MTJ-SET charge sensing device (electrometer). (a) SEM image of the fabricated memory, and (b) the corresponding circuit diagram. Reprinted with permission from [64]. Copyright 1998 American Institute of Physics.

be read as the current through a sense line. In addition to SETs and MTJ-SETs, which are known as sensitive electrometers, scaled-down MOSFETs are also sensitive enough to detect the presence of a single electron.

Apart from the floating-node types of memory described so far, there is another type called static memory. In static memory, small current flows through the memory node, there are multiple stability points in DC characteristics, and the data are retained as long as the power is on. One example of a single-electron static memory will be described at the end of the section.

3.2. Memories using a single-electron transistor as a sensing device

Figure 17 shows a memory having an MTJ electron trap and an MTJ-SET charge-sensing device, which was reported by Stone *et al* [64]. MTJs were fabricated in a doped Si wire as described in the latter part of section 2.1. The wire is made of SOI material with a dopant concentration of 1×10^{19} cm^{-3} and is 40 nm thick, 50 nm wide and 500 nm long. The device operated at 4.2 K and showed clear memory operation with a $>$100 mV gap between '0' and '1' levels. Roughly 30 electrons were estimated to tunnel into and out of the memory node during the transition between the two levels.

Another memory consisting only of SEDs was reported by Fujiwara *et al* [65]. Their device was fabricated by the PADOX process. It comprises a double-tunnel-junction electron trap and a SET charge sensing device, and one tunnel junction is shared by the trap and the SET. Operating at 30 K, the oscillatory conductance-versus-gate-voltage characteristics of the SET showed the hysteresis associated with multistability in the number of stored electrons.

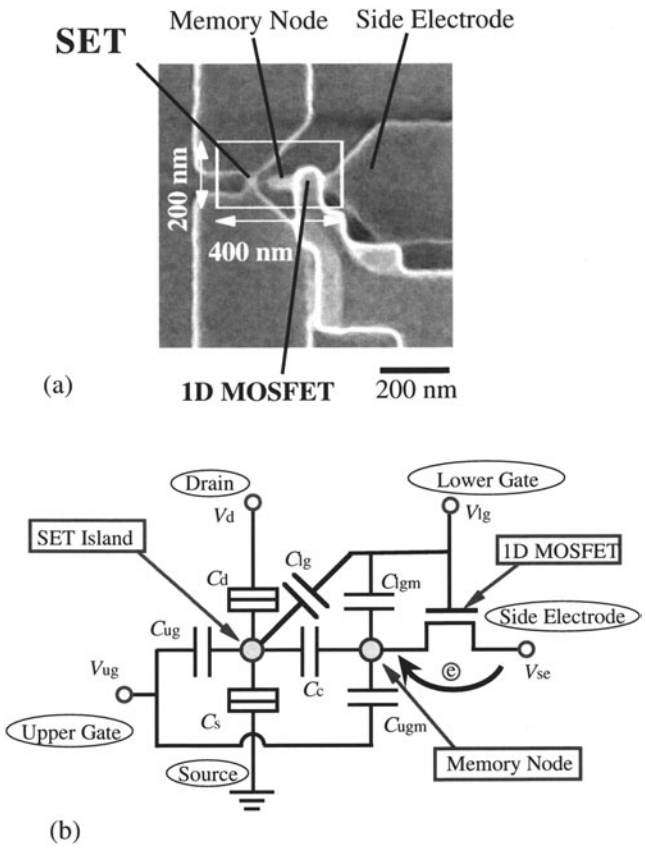

Figure 18. A memory with a write/erase MOSFET and a SET sensing device [67]. (a) SEM image of the fabricated memory, and (b) the corresponding circuit diagram.

A SET combined with a single-tunnel-junction electron box (nanocrystal on a tunnel oxide) has been reported by Takahashi *et al* [66], who claimed that this is useful in adjusting the peak position of a SET.

A SET sensing device was made together with a write/erase MOSFET by Takahashi *et al* [67]. Figure 18 shows the SEM image (a), and the corresponding circuit diagram (b). This particular device was fabricated by the PADOX process. The wire region of the SET was initially 100 nm long and 40 nm wide, and the memory node also had the same dimensions. The gate length of the MOSFET is 50 nm. Figure 19 shows the hysteresis characteristics of the SET current representing the 'write' and 'storage' actions at 40 K. Initially, at the lower-gate voltage V_{lg} of -2.7 V, the MOSFET cuts off and the storage node is not charged. As the V_{lg} increases, the SET current also increases due to the capacitive coupling between the lower gate and the SET island. When V_{lg} exceeds -2.4 V, the MOSFET channel becomes conductive and electrons flow into the memory node, lowering the potential of the CB island and causing a drop in SET current. Even after the V_{lg} is swept back to the initial -2.7 V, electrons are kept in the memory node and the charged state is clearly distinguished from the discharged state by the reduced SET current.

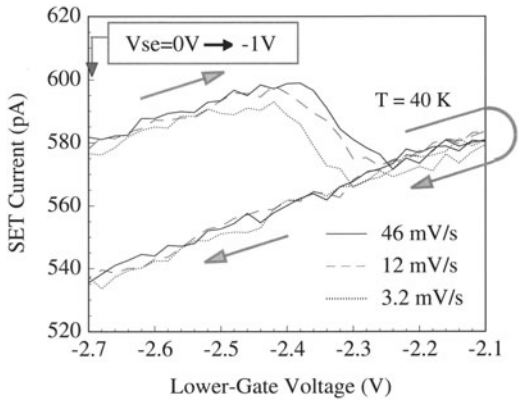

Figure 19. Hysteresis characteristics of the SET current representing the 'write' and 'storage' actions of the memory shown in figure 18.

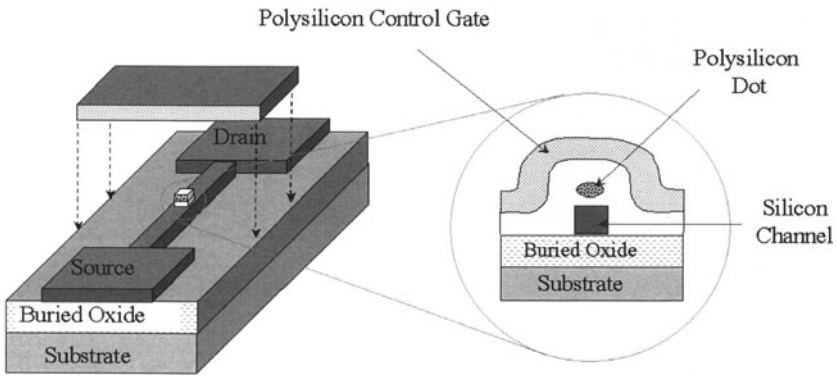

Figure 20. A single-dot memory comprising a narrow-channel silicon MOSFET and a nanoscale polysilicon dot (nanocrystal) as a memory node. Electron tunnelling occurs between the MOSFET channel and the polysilicon dot. Reprinted with permission from [68]. Copyright 1997 American Association for the Advancement of Science.

3.3. Single-dot memories with small MOSFET

The memories mentioned in section 3.2 operate mostly at low temperatures because of the difficulties in fabricating a small CB island for the charge sensing SET. Therefore, the use of MOSFETs is more realistic for room-temperature operation with current technologies.

The single-dot memory [68–70] is a combination of a single-junction electron box (figure 12(a)) and a MOSFET charge-sensing device. One refined example, which was reported by Guo *et al* [68], is shown in figure 20. A small ($\sim$7 nm $\times$ 7 nm in area and 2 nm thick) polysilicon dot is located just above a narrow ($\sim$10 nm) single-crystal MOSFET channel. Figure 21 shows the relationship between the threshold voltage and the control gate voltage. A quantized shift of threshold voltage, which can be attributed to the single-electron charging, is clearly observed at room temperature.

Yano *et al* [71, 72] utilized an ultrathin ($\sim$3 nm) polysilicon film to naturally form a single-dot memory (figure 22). In such a thin film, there is a large fluctuation in thickness and also in the electronic potential. As positive bias is applied to the gate, a narrow percolation channel and an isolated island appear where the potential is low, and they work as a memory.

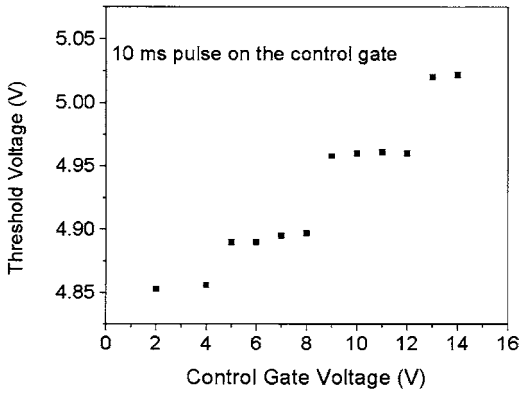

Figure 21. Write characteristics of the memory shown in figure 20 measured at room temperature. The threshold voltage changes as a function of the charging voltage on the control gate, showing a staircase-like relation with ∼4 V for each stair. Reprinted with permission from [68]. Copyright 1997 American Association for the Advancement of Science.

A discrete threshold voltage shift caused by the single-electron charging was observed at room temperature. They fabricated a 64-bit memory array to examine write/erase, retention and endurance characteristics. The write/erase time was typically 10 μs, resulting in data-transfer capability two orders larger than for typical flash memories. The retention time was typically 1 h to a month. Their memory showed high endurance against repeated write/erase cycles, i.e. there were no obvious changes in threshold voltages in write and erase states even after 10^7-cycle operation. They also showed the usefulness of the verify operation in compensating the device-to-device variation in the naturally formed structure. Their works showed the possibility of silicon-based SEDs at room temperature in the early 1990s, which stimulated other research in this field.

3.4. Multi-dot memories with MOSFET

Multi-dot memories consist of a large number of single-electron boxes (nanocrystals) that are separated from the sense MOSFET channel by a thin tunnel oxide (figure 23). Figure 24 shows the first demonstration by Tiwari *et al* [73, 74], in which a large threshold voltage shift is attained by a small write (charging) voltage. The discrete threshold voltage shift corresponding to the single-and multiple-electron storage was observed at 77 K. The thin tunnel oxide leads to the small write voltage, and is also expected to improve the endurance characteristics [75, 76] to the level of DRAM, i.e. more than 10^{10} cycles. The unexpectedly long retention time (e.g. more than one week at room temperature for 1.6 nm tunnel oxide), which might be a result of the storage of injected electrons in the deep trapping centres [77, 78], also encourages use as a nonvolatile memory. In contrast to the continuous large floating gate in conventional flash memories, the multi-dot memory is robust against defects in the oxide; only nanocrystals close to the defects are affected by them and almost all the stored charges remain unaffected.

Since the small size, the small size distribution [79] and the large density (total area) [80] of nanocrystals are important in achieving an effective CB, uniform charging and a large threshold voltage shift, respectively, many nanocrystal fabrication techniques have been investigated. Low-pressure CVD is the most common, but different underlayers, such as SiO_2, HF-treated SiO_2 [44], Si_3N_4 [81], oxynitride [82] and Al_2O_3 [83], have been examined. Others include remote-plasma-enhanced CVD [84], aerosol fabrication [85], annealing of silicon-rich

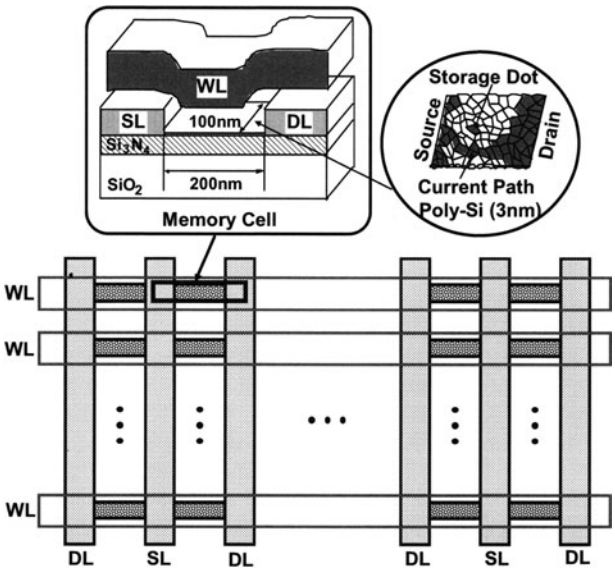

Figure 22. A single-dot memory having a dot and a narrow-channel MOSFET naturally formed in a ultrathin (∼3 nm) polysilicon layer. The ladder-shaped memory cell array consists of a word line (WL), data line (DL) and source line (SL), all made of polysilicon, and has a unit cell area of $6F^2$, where F is the feature size. Reprinted with permission from [72]. Copyright 1999 IEEE.

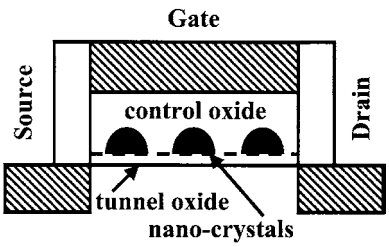

Figure 23. A multi-dot memory comprising a MOSFET and a large number of nanoscale dots (nanocrystals) as memory nodes. Electron tunnelling occurs between the MOSFET channel and the nanocrystal dots. Reprinted with permission from [73]. Copyright 1995 IEEE.

oxide [86], ion implantation of Si, Ge or Sn into SiO_2 followed by annealing [87, 88] and Ge implant into Si followed by oxidation [89].

Despite intensive research on the multi-dot memory, it is still quite ambiguous whether this memory can replace DRAM or flash memory in the future. Attaining the short write/erase time of DRAM (∼10 ns) at low voltage seems difficult, as does attaining the long retention time (>10 years) and the high endurance ($>10^5$ cycles) of flash memory using a tunnel oxide thin enough to be compatible with scaled-down MOSFETs.

One approach to relaxing the trade-off between write/erase and retention times is the use of a double- or multiple-tunnel-junction electron trap (figures 1(b) or (c)). Ohba *et al* [90] fabricated doubly stacked dots in a self-aligned manner, and observed improved retention. But further optimization of the device structure is still needed to verify the overall merit of this scheme.

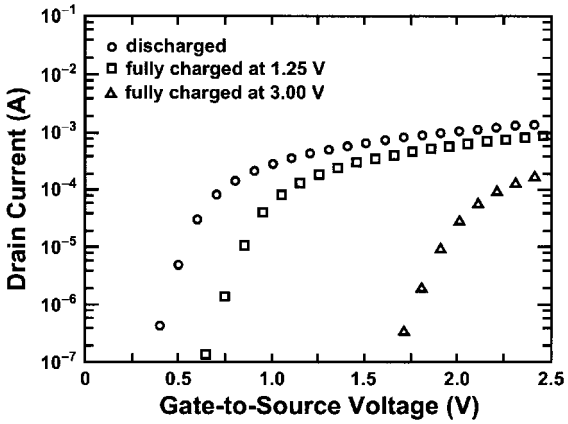

Figure 24. Drain-current–gate-voltage characteristics of the memory shown in figure 23. This example uses a 1.6 nm tunnelling oxide, a ∼5 nm nanocrystal with a density $<10^{12}$ cm^{-2} and a control oxide of 7.3 nm. The left curve corresponds to the case with no electron in the dot, the middle one to one electron per dot and the right curve to four to five electrons per dot. Reprinted with permission from [73]. Copyright 1995 IEEE.

3.5. Other memories including single-electron devices

In the tradition of DRAM, a combination of a write/erase MOSFET (figure 12(d)) and a sense MOSFET (figure 13(a)) is called a 'gain cell' [62, 63]. Since the charges in the storage capacitor are not directly shared by the bit-line capacitance in read operation, the difficulty in obtaining a large storage capacitance is avoided. Although the gain cell has been expected as a memory for future generations, it has been very difficult to make a write/erase transistor with a minimal leakage current *and* a small area. Now, SEDs offer a way to meet this challenge.

Figure 25 shows a gain cell with an MTJ trap and a MOSFET fabricated by Durrani *et al* [91, 92]. Although the memory node is shrunk to 1 μm $\times$ 70 nm and the stored charge is reduced to 30 electrons, cell area is still large. In addition, suppression of the leakage current is insufficient, resulting in the maximum operating temperature of 65 K.

The phase-state low-electron-number drive transistor (PLEDTR) [93, 94] and single-electron shut-off (SESO) transistor [95] are also intended for use as write/erase transistors in gain cells. They are more advanced in view of their small cell area (4–6F^2, where F is the feature size), room-temperature operation and small leakage current (experimentally <1 fA and 1.1×10^{-19} A, respectively). However, the PLEDTR is a kind of heterostructure hot-electron diode [96], despite it having a layered structure similar to the MTJ. A SESO transistor is actually an FET with an ultrathin (∼2 nm) polysilicon channel, and, unlike Yano's single-electron memory (figure 22), does not have a memory effect by itself. Though the single-electron charging effect does not seem to play an important role in these two transistors, gain cells with them may be called single-electron or few-electron memories considering the small number of electrons stored in the memory node.

Figure 26 shows a multiple-valued static memory comprising a SET and a MOSFET [97]. The operating principle is completely different from that of floating-node-type memories, but can be easily understood by regarding the SET and the MOSFET as circuit elements. The MOSFET here keeps the SET drain voltage constant at a low enough value. As a result, the current flowing through the circuit is determined only by the SET input voltage; it is not affected by the output voltage. When the input and output terminals are shorted together, multipeak

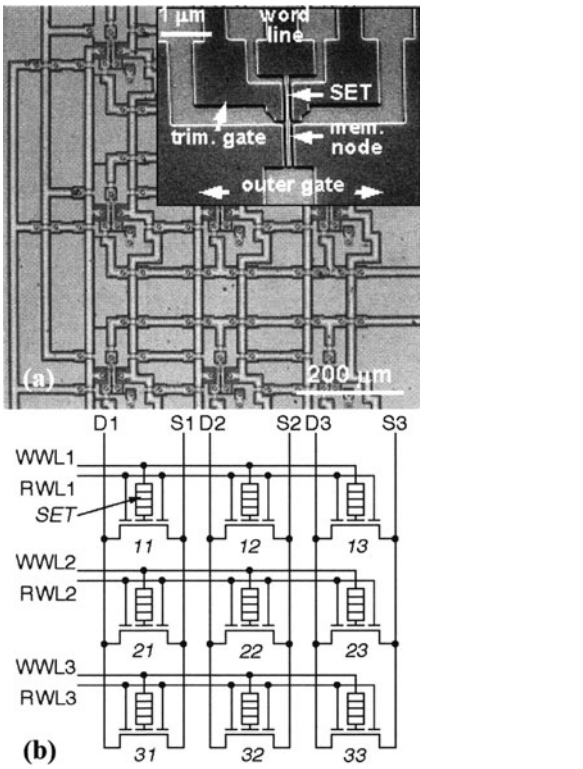

Figure 25. A memory with an MTJ electron trap and a MOSFET sensing device. (a) Optical micrograph of a 3 × 3 array of memory cells, and (b) the corresponding circuit diagram. Reprinted with permission from [91]. Copyright 2000 IEEE.

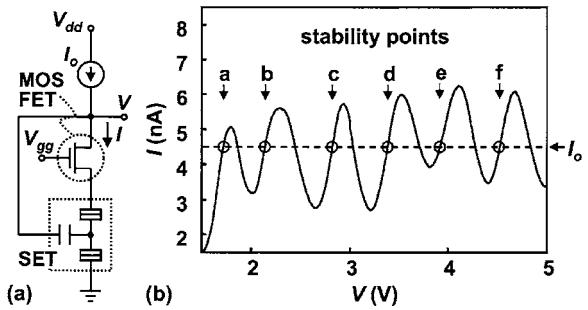

Figure 26. Multiple-valued static memory comprising a SET and a MOSFET [97]. (a) Circuit diagram and (b) multipeak negative-differential-resistance characteristics measured at 27 K and the stability points corresponding to the constant-current load of 4.5 nA.

negative differential resistance is attained as two-terminal characteristics. With a proper load device (a constant-current source in the case of figure 26), many stability points appear and this circuit works as a multiple-valued memory. This particular device was fabricated by the PADOX process and operated at 27 K. Static memories, which feature fast and simple write operation and stable retention, will have an application field different from that of floating-node-type memories.

Silicon single-electron memories are close to becoming a reality thanks to the compatibility with CMOS LSI technology. Since a genuine single-electron memory that deals with only one electron is severely affected by random offset charges [4], multiple-electron storage in a node or multiple nodes in a cell (like a multi-dot memory) would be the proper choice. Overcoming the scaling limit of flash memory and DRAM by the use of SEDs is anticipated.

4. Single-electron logic

In contrast to memory, logic allows a quite rich and large variety of system architectures and circuit designs. Consequently, many methods of computation have been proposed and analysed for SEDs. Some of them resemble *logics used in CMOS digital technology* [8, 98–117]. The major advantage of this type is that we can employ the accumulated full-fledged technologies for CMOS circuit designs. (However, they are not copies of the CMOS logic.) The principal device is the SET, which is used as a substitute for the MOSFET. Although the circuit characteristics are predominated by the CB and single-electron tunnelling, these phenomena are not directly employed for computation; we use the current produced by the sequence of single-electron tunnelling and the bit is represented by the voltage generated by the accumulation of plural electrons. We here call this SET-based logic. A second type comprises *logics that use an elementary charge for bit representation* [118–129]. These are highly specific to SEDs and might be in some sense the ultimate logics. SEDs other than SETs, such as the single-electron pump, are building blocks. We here call such logics charge state logic. There are other types of computational method. One uses the phase of single-electron-tunnelling oscillations for bit representation [130] and another applies the stochastic nature of the single-electron tunnelling to analogue computing or neural networks [131–133]. Although these are interesting because they might provide some sort of fault tolerance in the circuits, they are not discussed in this section because of a lack of experiments.

SET-based logic is being intensively studied in Si-based research, and some fundamental circuits, such as inverter, NAND and XOR gates, have already been demonstrated. Such studies are described in section 4.1 in relative detail. Experiments on charge state logic have mainly been conducted using metal-based SEDs, but recently Si-based research has begun. We will touch on such efforts in section 4.2.

4.1. Single-electron-transistor-based logic

We can define the voltage gain of the SET [8]. This parameter is explained using the electrical characteristics of a SET shown in figure 27(a). Figure 27(a) shows the output drain voltage V_d for a fixed input drain current I_d, as a function of the gate voltage V_g, for a SET made by V-PADOX. The output voltage exhibits the Coulomb diamond. We can define noninverting/inverting voltage gain G_{ni}/G_i as the slope of the rising/falling side of the diamonds. These gains are expressed as

$$G_{ni} = C_g/(C_g + C_j) \tag{3}$$

$$G_i = C_g/C_j \tag{4}$$

where C_g and C_j are the gate and junction capacitances, respectively [8, 105]. As can be seen in equations (3) and (4), the inverting gain can exceed unity by making C_g larger than C_j, while the noninverting gain can never do so. This means that we can make inverters that can amplify voltage (and also power) and logic circuits can be constructed based on the inverters, just like CMOS logic. Since, unlike the MOSFETs, SETs have no saturation region in their I_d–V_d characteristics, making G_i high is important for logic applications. However,

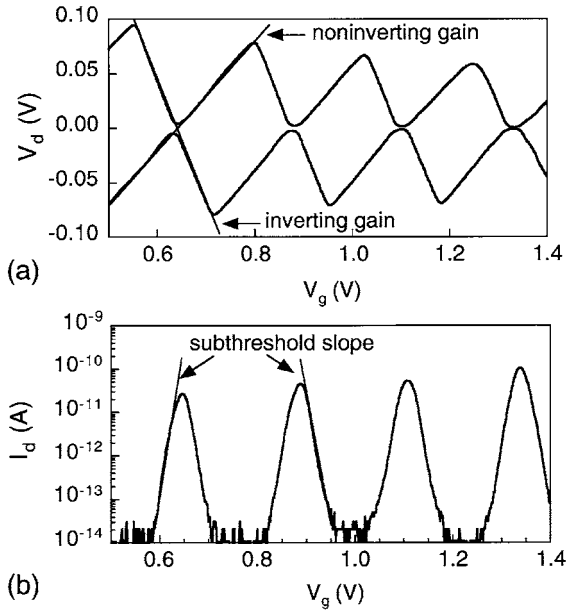

Figure 27. Electrical characteristics of a SET made by the V-PADOX process [138]. (a) The output drain voltage V_d for a fixed drain current I_d of ± 10 pA and (b) the output drain current for a fixed drain voltage V_d of 10 mV. The measurement temperature was 27 K.

making C_g larger for higher G_i leads to a larger total capacitance. Therefore, voltage gain and operation temperature are in a trade-off relationship and it is not so easy to make SETs with larger-than-unity gain operating at high temperatures. Although G_i larger than unity has been achieved in metal-based [134, 135], GaAs-based [136] and Si-based SETs [137], they operate at temperatures below 4 K. However, the V-PADOX process has enabled us to make SETs with voltage gain as high as four at around 30 K [138].

We can also define the subthreshold slope S because peaks in I_d–V_g characteristics rise and fall nearly exponentially at their tails. This parameter is indicated in figure 27(b), where the output drain current I_d for a fixed input drain voltage V_d is plotted as a function of V_g in a logarithmic scale. Given sufficiently low temperature and high tunnel resistance,

$$S = [\mathrm{d}(\ln I_d)/\mathrm{d}V_g]^{-1} = mkT/e, \tag{5}$$

where $m = C_\Sigma/C_g$ with C_Σ of the total capacitance of the island [105, 113]. We can express $m = 1 + 2/G_i$, given $C_\Sigma = C_g + 2C_j$, and recognize that the high voltage gain is important in order to obtain a small S as well. The voltage gain of 4 comes to m of 1.5, which is comparable to the value for conventional MOSFETs.

An additional and significant feature of SETs is that they can have plural gates. As in a neuron MOSFET [139], such a multigate configuration enables us to generate sum-of-product at the gate input level. In contrast to the neuron MOSFET, however, SET multigates can directly couple to the island and thus need no floating gates that cause unwanted charging and discharging. This is an advantage. The combination of the multigate configuration and the unique peak-and-valley structure in I_d–V_g characteristics makes the SETs highly functional. For simplicity, we will explain what a double-gate SET can do.

One way to exploit the double-gate configuration is to use one of the gates for control of the electrical characteristics (thereby called control gate) and the other for input. As shown in

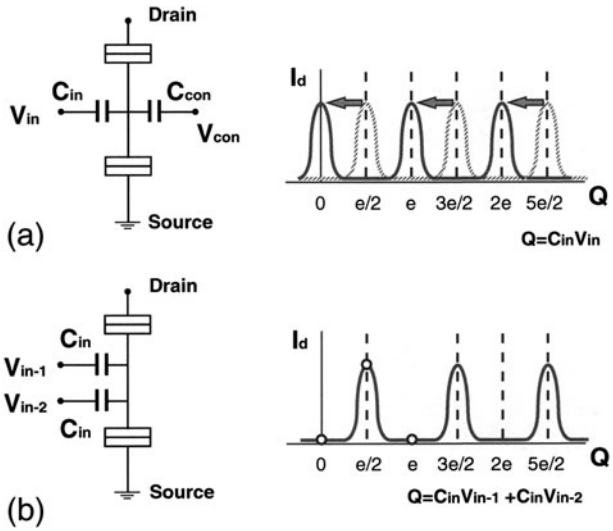

Figure 28. Equivalent circuits and current curves of double-gate SETs. In (a), V_{in}, V_{con}, C_{in} and C_{con} are the input-gate voltage, control-gate voltage, input-gate capacitance and control-gate capacitance, respectively. Solid and dashed curves are drain current I_d for $V_{con} = e/C_{con}$ and 0, respectively, as a function of external charge Q to the input gate. In (b), $V_{in\text{-}1}$ and $V_{in\text{-}2}$ are the voltages applied to the two input gates. Open circles in the current curve are operation points for the XOR gate.

figure 28(a), when the control gate is positively biased by $e/2C_{con}$ where C_{con} is the control gate capacitance, the I_d–V_g curve shifts by 180° to the negative V_g direction. In such a case, a peak is positioned at zero input-gate voltage or the switching characteristics are reversed. The relationship between the biased SET and unbiased one is similar to that between p- and n-MOSFETs. Therefore, their combination enables us to construct complementary logic on a single type (n- or p-type) of substrate. This property was first discussed by Tucker [98], and was actually employed in a complementary inverter, which will be explained later.

Another way to exploit the double gates is to use both gates as input gates (figure 28(b)). Provided the two input-gate capacitances are the same and the gate input amplitude is $e/2C_{in}$, where C_{in} is the input-gate capacitance, the SET is ON only when one of the inputs is HIGH, and the SET is OFF when neither or both inputs are HIGH. This function is XOR. This SET XOR gate [103, 106] is powerful when we construct arithmetic units like adders and multipliers because XOR is nothing other than what we call half-sum, which is the lower order bit calculated by adding two one-bit binary numbers. The XOR gate was also experimentally demonstrated using a Si dual-gate SET made by PADOX [140]. Figure 29(a) shows a SEM image of the dual-gate SET. The XOR function was confirmed in an output drain current at 40 K, as shown in figure 29(b).

4.1.1. Resistively loaded and complementary logics. The simplest SET-based logic is the one that uses single-gate SETs and resistive loads [102]. Nishiguchi *et al* fabricated an inverter based on this logic on a SOI wafer [141]. The SET consists of a small Al island made by evaporation using a self-alignment technique, and two leads made of the SOI layer. Larger-than-unity gain was achieved at 5 K, though the logic swing was small.

Based on the SET complementary logic [98, 102], two inverters were independently fabricated. One is Si based [142] and the other Al based [143]. The Si-based inverter was

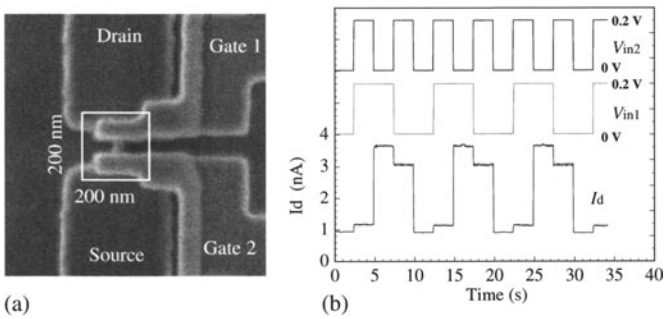

Figure 29. (a) SEM image of a dual-gate SET made by PADOX and (b) experimental demonstration of the XOR operation at 40 K [140].

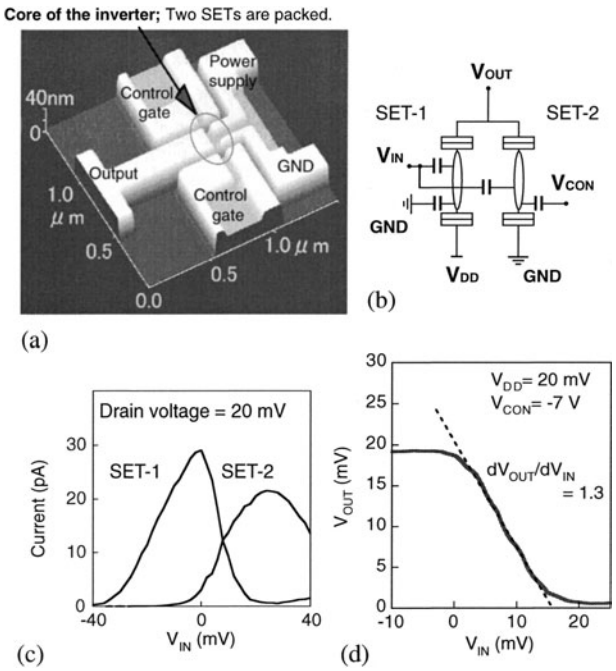

Figure 30. (a) AFM image and (b) equivalent circuit of the inverter fabricated using the V-PADOX process. The input gate (not shown in (a)) covers two SETs. (c) Current characteristics of the SETs and (d) input–output transfer curve, measured at 27 K [142].

fabricated using the V-PADOX process. Figure 30 shows an AFM image, equivalent circuit, current curves for the two SETs and input–output transfer characteristics of that inverter. The two SETs with voltage gain of about two were packed in a very small (100 nm × 200 nm) area. The input and output transfer curve attains both larger-than-unity gain and full logic swing at 27 K. The Al-based inverter also attained a high voltage gain (∼2.6) but at a lower temperature of 25 mK. A NAND gate was also reported by Stone and Ahmed [144]. This was fabricated on an SOI wafer, on which four MTJ-SETs were integrated. The fundamental operation was achieved at 1.6 K, though the voltage gain was lower than unity.

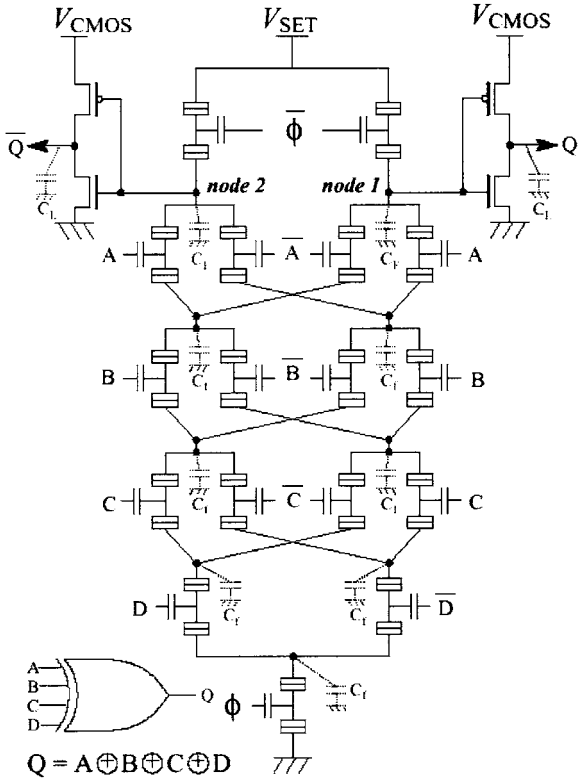

Figure 31. Example of circuits based on domino-type logic; four-way XOR; reprinted with permission from [111]. Copyright 1999 Japan Society of Applied Physics.

4.1.2. Domino-type and pass-transistor logics. As we have pointed out, it is not easy to obtain high voltage gain using SETs. The CMOS-domino-type logic was proposed by Uchida *et al* [111] as a way to compensate for this drawback. A combinational logic circuit is built in a SET logic tree, where SETs are used as pull-down transistors. The point is that the tree is operated with a sufficiently small excitation voltage (or drain voltage) in order to make the CB effective. The output signal with such a small voltage is then amplified before transfer to the next logic segments. The report also emphasized the importance of the combinational usage of SETs and MOSFETs. Figure 31 shows an example of circuits based on such a concept. CMOS inverters are used for amplifiers. The building block for the logic is a directional current switch composed of two single-gate SETs. Such a current switch has been fabricated on SOI substrates and its function was confirmed at around 30 K [28, 145, 146]. Also, basic logic operation, such as NAND, was performed using this scheme at 10 K [38].

The single-electron pass-transistor logic, where SETs are used both as pull-up and pull-down transistors, has also been studied. An elemental circuit of the single-electron pass-transistor logic was fabricated using V-PADOX, and half-sum and carry-out for the half adder has been demonstrated at 25 K [147]. Figure 32 shows the measurement data. Both half-sum and carry-out are correctly output at 25 K. The significance is that the gate and total capacitances, and even the peak positions of the fabricated SETs, were well controlled for these operations. This is the first arithmetic operation by SET-based circuits.

There have been some attempts to build circuits that can change their functions reconfigurably by combining SETs and quantum-dot memory. In such a scheme, the floating

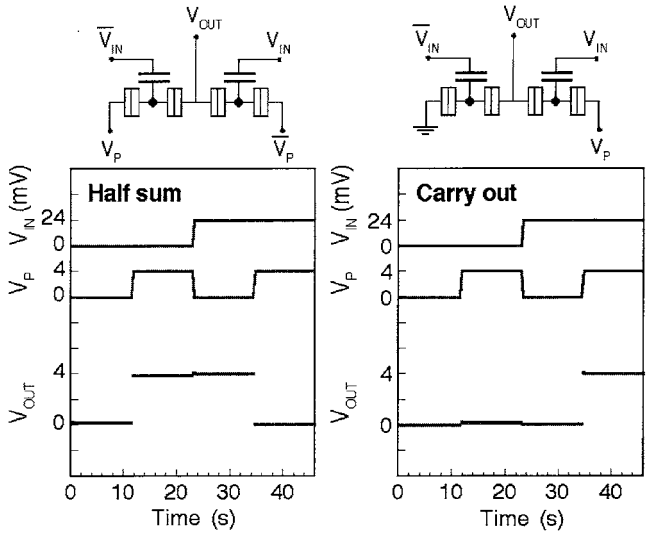

Figure 32. Experimental data of one-bit sum and carry-out performed at 25 K, based on pass-transistor logic scheme [147].

dots are used as alternatives of the control gate for controlling the position of current peaks. Fundamental operation has been confirmed using a circuit composed of two SETs [146] and a SET/MOSFET hybrid circuit [148]. Integrated circuits comprising these components should also be operated based on the domino-type or pass-transistor logic.

Although the single-gate SETs is good enough for the domino-type and pass-transistor logics, multigate SETs are also acceptable. Since the gate capacitance is shared by plural gates in the multigate configuration, obtaining a high voltage gain is more difficult than in the single-gate configuration. Therefore, this type of logic is crucial for multigate SETs. It was shown that the combination of multigate SETs and pass-transistor logic enables us to construct full and multibit adders in a very compact way [117]. However, circuits based on the idea have not yet been fabricated.

4.1.3. Multiple-valued and majority logics. Multiple-valued logics have potential advantages over binary logics with respect to the number of elements per function and operating speed [149, 150]. They are also expected to relax the interconnection complexity on the inside and outside of integrated circuits. However, their success has been limited, partially because the devices used (MOSFETs and negative-differential-resistance devices like resonant tunnelling diodes) are inherently single threshold or single peak, and are not fully suited for multi-valued logic. The oscillatory behaviour in I_d–V_g characteristics suggests that SETs be used in the multiple-valued scheme. Several methods have been proposed for SET-based multiple-valued logic circuits [110, 151–153]. One is the merged SET–MOSFET configuration described in section 3 for multiple-valued memory. Using this configuration, it is possible to create a considerably large multiple value using only one SET. Actually, Inokawa *et al* [151] fabricated a literal gate and a quantizer using PADOX and demonstrated their operations at 27 K. Figure 33 shows the measurement setup for the quantizer and its measurement data. The triangular input V_{IN} was successfully quantized into six levels. It should also be noted that a low voltage gain of the SET can be remarkably amplified in this configuration [152].

Another way to realize the multiple-valued logic is to use the SET XOR gate. A T-gate and modsum was proposed based on this configuration [153]. As has been pointed out, the multigate

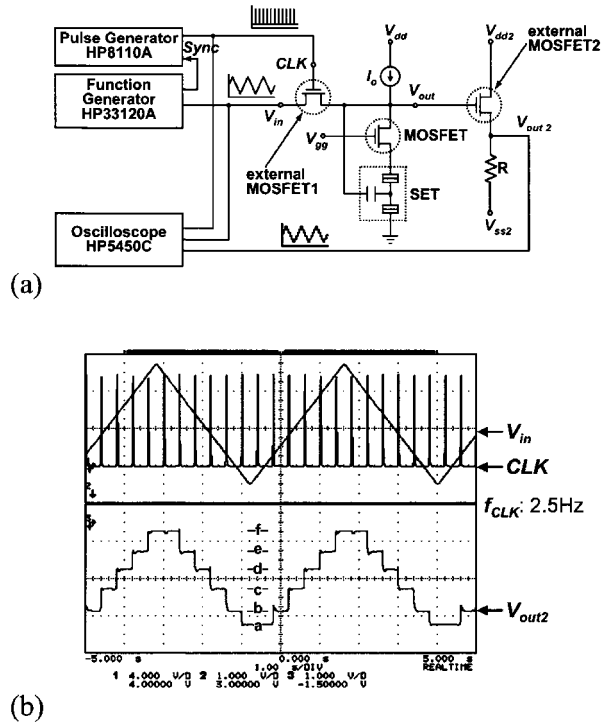

Figure 33. Quantizer made by PADOX [151]. (a) Measurement setup and (b) measurement data at 27 K.

configuration produces sum-of-product at the gate-input level. Therefore, circuits based on the majority logic can be constructed [107]. Although the XOR demonstrated experimentally had only two inputs, it is conceptually possible to have larger number of gates, and up to six gates will be achievable with the current lithography technology for SETs operating at around 40 K [140]. However, there are no reports of the fabrication of circuits based on the multiple-valued logic or majority logic using multigate SETs.

4.2. Charge state logic

This logic uses single electrons (or holes) to express bit information, and can be classified into two types. In one of them, the computation is carried out by controlling the distribution of excess electrons over the entire circuit (or polarization of the circuit) using external bias, which can be electric fields or extra charges [118–122]. The goal of this type of logic is to achieve extremely low power dissipation by constructing a no-metal-interconnection configuration to overcome the interconnection bottleneck of current CMOS LSIs. The representative is the quantum cellular automaton (QCA) [118–120]. QCA circuits comprise regular arrays of quantum dots. Because of the capacitive coupling and finite tunnelling rate between adjacent dots, an external bias changes *the pattern* of the distribution of the dots that contain an extra electron, and the final pattern of the global equilibrium state corresponds to the computation result. The other type conveys a single electron from a certain point to another in the circuit by using clock signals or an external DC voltage [123–129]. The representative is the single-electron binary decision diagram (BDD) [127]. The BDD was originally proposed for the

circuit design of MOS-LSIs [154]. When we apply this method to single electron circuits, we use a single electron as a *messenger* and convey it in a logic tree. The route is selected by clock signals applied to gates, which are attached to each segment of the tree. Therefore, this logic closely resembles pass-transistor logic, but the number of electrons flowing through the pass signal route is exactly one in the single-electron BDD.

At present, QCA is the only one whose logic elements have been experimentally verified [155] (but not based on Si). No circuits have been fabricated based on the single-electron BDD, although a similar logic, in which a bunch of electrons instead of a single electron are transferred, has been tested [156, 157]. The main experimental efforts in this field are focusing on how to fabricate base devices rather than circuits for both types (QCA-like and BDD-like) of logic.

The base device for logic is called the single-electron charge-transfer device. The possibility of elementary charge transfer was discussed at a very early stage [158–160], and several devices have so far been proposed and tested [161–168]. Some of them are based on single-electron tunnelling. The single-electron turnstile [161] and single-electron pump [162–165] are included in this category. They comprise sequentially connected multiple (at least two) islands, and electrons are transferred from island to island one by one, which is regulated by AC bias applied to gate(s). The SET is also capable of manipulating single electrons. Although the tunnelling event in SETs is inherently stochastic, its regulation is possible by modulating tunnelling rate using AC bias [166]. The other type of device utilizes a potential dip for positioning single electrons, which are conveyed by moving the dip. The surface acoustic wave device [167] and charge-coupled device (CCD) [4, 168] are included in this category. All of these devices have been experimentally demonstrated but mainly they have been metal-based and GaAs-based devices. The exception is the CCD, which was demonstrated originally and only in Si [168].

Attempts to make sequentially connected double islands have been made using SiGe [169, 170] and undoped and doped SOIs [145, 171, 172]. Single *et al* [172] fabricated a pair of such double-island devices on a phosphorus-doped SOI. Figure 34 shows the top view of these devices. The upper two islands, marked t1 and t2, and two side gates, t5 and t6, constitute one double-island device, while the lower two islands, b1 and b2, and side gates, b5 and b6, constitute another. Figure 35 shows the measured stability diagram in the gate-voltage plane for each device. The two diagrams exhibit similar characteristics within the regions indicated by the broken lines. This indicates that each double-island structure was made in a controlled way. The present configuration, i.e., two sequentially connected double-island structures positioned close to each other, can be the basic cell of QCAs if the capacitive couplings between t1 and b1 and between t2 and b2 are strong.

A single-electron turnstile and pump have not yet been fabricated using Si-based materials. We should however notice that the transfer of a bunch of (not a single) electrons, which was first demonstrated using GaAs-based MTJ devices [156, 157], has been tested in Si [173]. SETs have a rectifier property for AC drain bias [174] because of their asymmetric drain-current versus drain-voltage characteristics, and the electron transfer demonstrated relies on this rectifier property.

To our knowledge, single-electron transfer in Si was first observed not using an active device but using an interface trap at a SiO_2/Si interface. Saks *et al* performed charge pumping experiments on small MOSFETs, and observed a quantized current ef with f of charge-pumping frequency [175]. They ascribed the quantized current to single electrons trapped in an interface defect. Single-charge manipulation in Si has only been achieved by the CCD [168]. The CCD does not require tunnel barriers because the charge is trapped in an electrically driven potential dip. This makes the fabrication easy, which is one of the important features of the

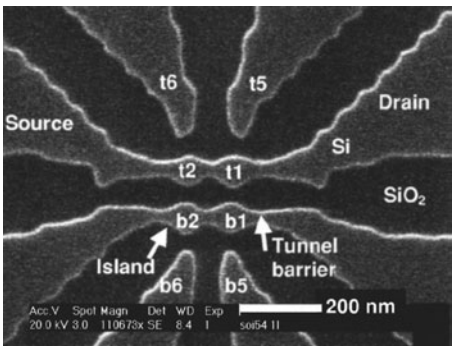

Figure 34. SEM image of two closely positioned double-island devices fabricated on a SOI substrate. Reprinted with permission from [172]. Copyright 2001 American Institute of Physics.

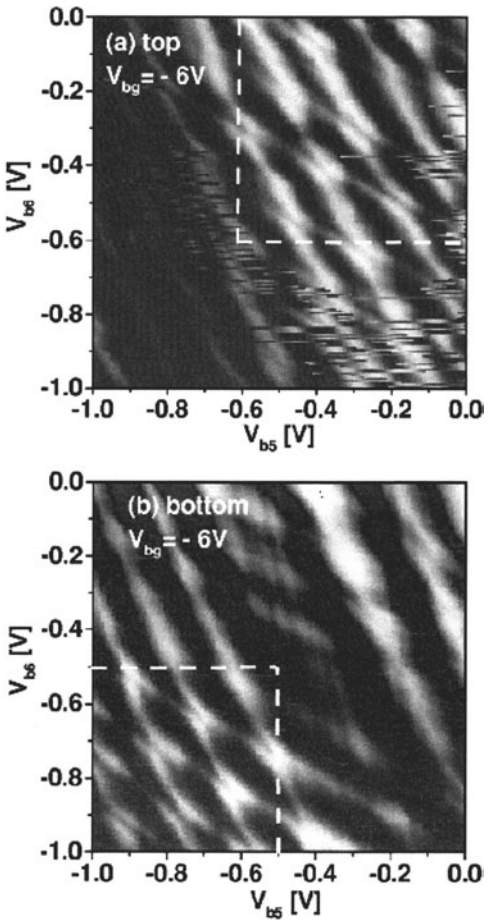

Figure 35. Electrical characteristics of the (a) top and (b) bottom device. The measurement temperature was 4.2 K. The brighter regions correspond to the higher-current-level regions. Reprinted with permission from [172]. Copyright 2001 American Institute of Physics.

device. Fujiwara and Takahashi demonstrated this device. They first developed techniques for generating a single charge and for sensing it. These techniques are based on control of the generation and recombination of electron–hole pairs, which was originally investigated in a PADOX SET [176], and then applied to Si wire MOSFETs for the CCD [177]. The idea is that a single hole generated by illumination is sensed, before recombination occurs, by electron current flowing near the hole and vice versa. Figure 36(a) shows a schematic diagram of the CCD, which is a closely packed array of two Si-wire MOSFETs with individual drains and a common source. A single hole can be stored under either of these MOSFET gates. Figure 36(b) shows the demonstration of single-hole transfer at 25 K. The transfer was done by changing the bias voltage of each MOSFET, and the presence and absence of the hole was checked by monitoring the level of the sensing electron current flowing through each MOSFETs. Recently, the sensing of single charges has been demonstrated even at room temperature for both electrons and holes [178], which suggests the possibility of room-temperature operation of the single-electron CCD.

5. Summary

Si SEDs are widely investigated as memory and logic devices to attain higher levels of integration. One of the main reasons is their small size, which is especially important for memory devices; memory cells must be small. Many works have been done by using multi-dot memory structures to overcome the scaling limit of DRAMs and flash memories, which will become a problem in the near future. At present, there is no strong necessity for a genuine single-electron memory that can deal with only one electron because power dissipation in a memory is not a critical problem and there is an adverse effect in small-charge storage. It is a memory for the future that will be used with a defect-tolerant scheme.

The low-power-dissipation nature of SEDs will be usable for logic LSIs. Many kinds of application have been proposed and some of their basic operations have been demonstrated at low temperatures. Room-temperature operation is the most critical issue for practical applications. For this, advances in lithography that will enable us to make a pattern smaller than 10 nm with high accuracy are needed. The 2001 edition of ITRS (International Technology Roadmap for Semiconductors) predicts this will become possible at around 2015. Considering that actual miniaturization is occurring faster than ITRS predicts, and that ITRS is revised every year, a more positive outlook is that sub-10 nm size will be achieved before 2010. Another important issue in single-electron LSIs is how to use SEDs. Although one of the biggest advantages of SEDs is their low-power nature, we should also use the other unique features of SEDs to achieve functionality higher than conventional CMOS devices, which would allow us to make circuits efficiently. The multigate configuration, multi-peak (oscillatory) characteristics and stochastic transport are completely different features and usable for implementing complicated functions with a small number of devices.

The logic circuit configurations of the far future might be completely different from the one that we are now investigating, and some new materials, such as C_{60}s, carbon nanotubes and DNAs, might be introduced to constitute so-called molecular electronics. Nonetheless, Si-based studies are still important because they can help us bridge the gap between current CMOS LSIs and future molecular LSIs. We have to connect the molecular world with the real world by some means, which will most likely be Si SEDs. We should also point out that even when we establish the technologies that can control molecules, significant reductions of power dissipation cannot be expected as long as the circuits use simple switches in computational architectures similar to current CMOS LSIs. It is important to accomplish the evolution in architectures. In achieving this, SEDs will be key components. Future circuits should have

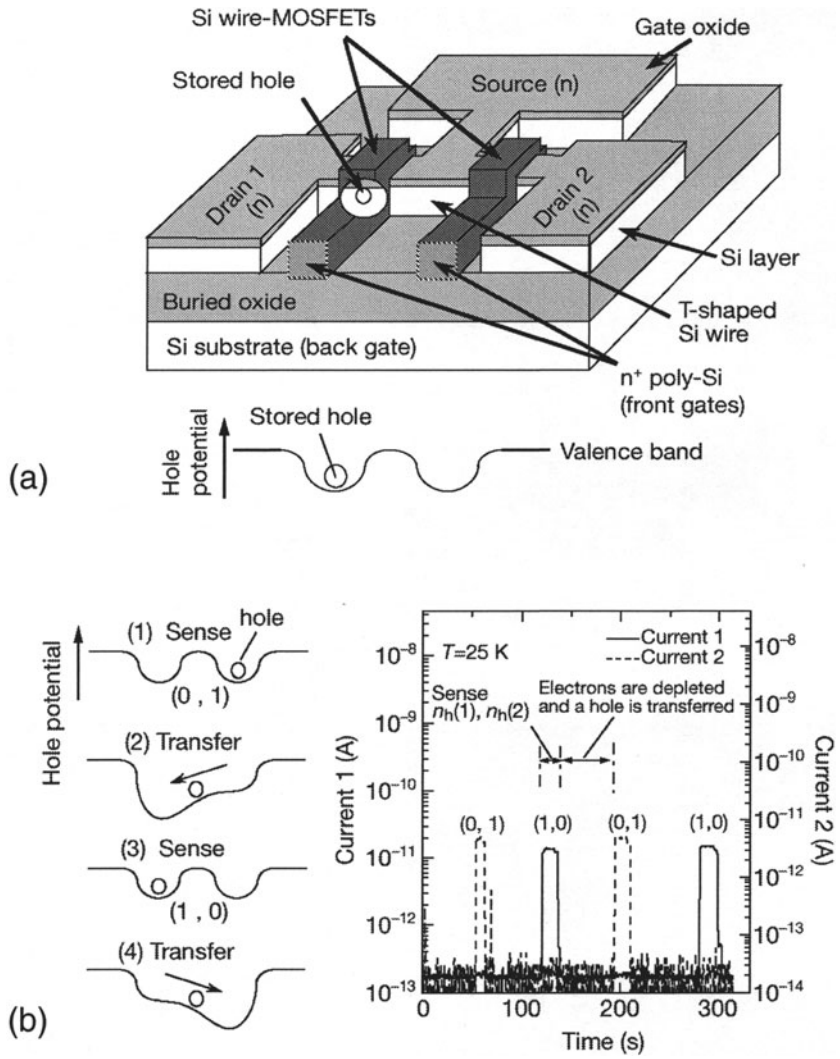

Figure 36. (a) Schematic view of the CCD and (b) demonstration of a single-hole manipulation [168].

redundancy, such as neural networks or fuzzy logic, because it will be difficult to keep testability due to too large integration levels. It is well known that many more transistors are needed in order to achieve redundant circuits. Consequently, individual devices should be low power. In addition, the stochastic transport characteristics and multigate capability of SEDs are expected to be usable in creating new redundant circuits that are still in the research phase.

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